19-5111; Rev 1; 7/10

EVALUATION KIT AVAILABLE

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

General Description

The MAX97002 mono audio subsystem combines a mono speaker amplifier with a stereo headphone amplifier and an analog DPST switch. The headphone and speaker amplifiers have independent volume control and on/off control. The 4 inputs are configurable as 2 differential inputs or 4 single-ended inputs.

The entire subsystem is designed for maximum efficiency. The high-efficiency, 700mW, Class D speaker amplifier operates directly from the battery and consumes no more than 1µA in shutdown mode. The Class H headphone amplifier utilizes a dual-mode charge pump to maximize efficiency while outputting a ground-referenced signal that does not require output coupling capacitors.

The speaker amplifier incorporates a distortion limiter to automatically reduce the volume level when excessive clipping occurs. This allows high gain for low-level signals without compromising the quality of large signals.

All control is performed using the 2-wire I²C interface. The MAX97002 operates over the extended -40°C to +85°C temperature range, and is available in the 2mm x 2.5mm, 20-bump, WLP package (0.5mm pitch).

Applications

Cell Phones

Portable Media Players

Features

- ♦ 2.7V to 5.5V Speaker Supply Voltage
- ♦ 1.6V to 2V Headphone Supply Voltage
- ♦ 700mW Speaker Output (V_{PVDD} = 3.7V, Z_{SPK} = 8Ω + 68µH)
- ♦ 37mW/Channel Headphone Output (R_{HP} = 16Ω)
- ♦ Low-Emission Class D Amplifier
- ♦ Efficient Class H Headphone Amplifier
- ♦ Ground-Referenced Headphone Outputs
- ♦ 2 Stereo Single-Ended/Mono Differential Inputs
- ♦ Integrated Distortion Limiter (Speaker Outputs)
- ♦ Integrated DPST Analog Switch
- ♦ No Clicks and Pops
- ♦ TDMA Noise Free
- ♦ 2mm x 2.5mm, 20-Bump, 0.5mm Pitch WLP Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX97002EWP+	-40°C to +85°C	20 WLP

Simplified Block Diagram

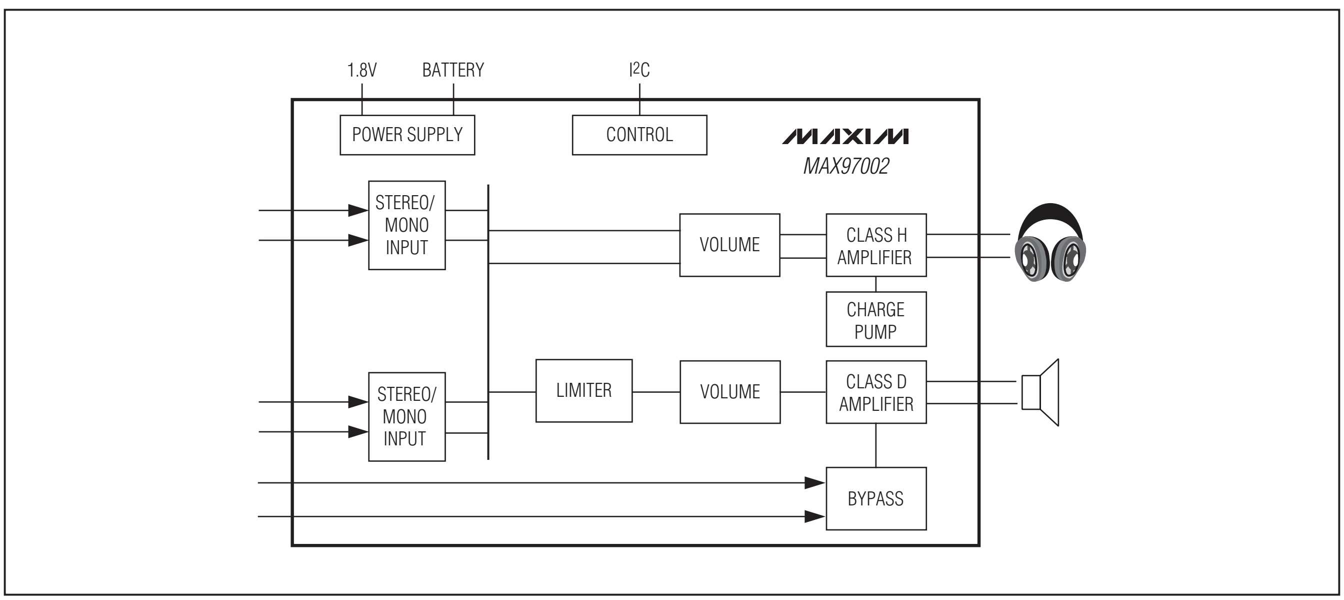
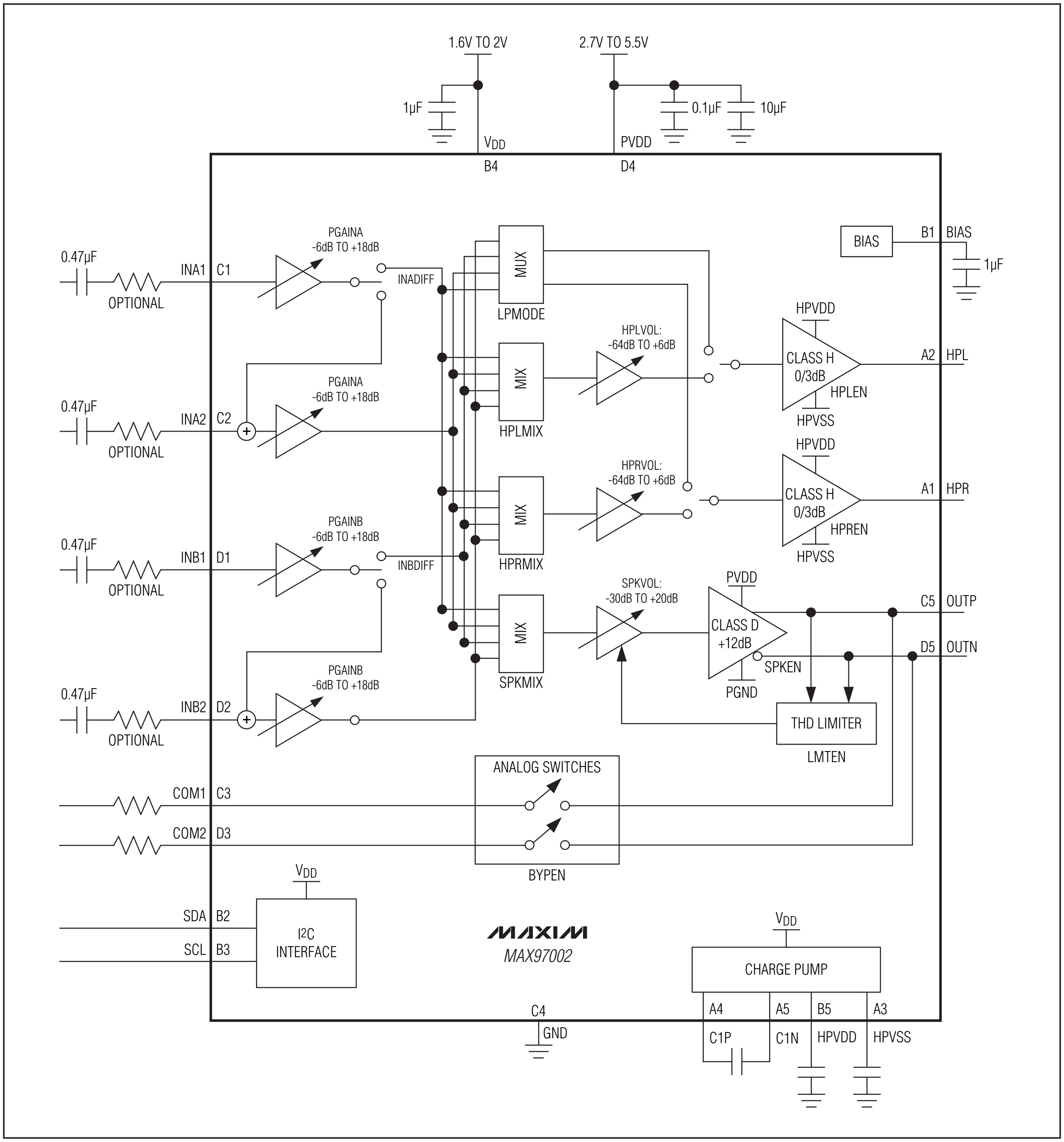


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Functional Diagram/Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to GND.)

V_{DD}, HPVDD ....-0.3V to +2.2V
PVDD ....-0.3V to +6.0V
HPVSS ....-2.2V to +0.3V
C1N ....(HPVSS - 0.3V) to (HPVDD + 0.3V)
C1P ....-0.3V to (HPVDD + 0.3V)
HPL, HPR ....(HPVSS - 0.3V) to (HPVDD + 0.3V)
INA1, INA2, INB1, INB2, BIAS ....-0.3V to +6.0V
SDA, SCL ....-0.3V to +6.0V
COM1, COM2, OUTP, OUTN.................-0.3V to (PVDD + 0.3V)
Continuous Current In/Out of PVDD, GND, OUT_ .... ±800mA
Continuous Current In/Out of HPR, HPL, V_{DD}............. ±140mA
Continuous Current In/Out of COM1, COM2 .... ±150mA
Continuous Input Current (all other pins)........................ ±20mA
Duration of OUT_ Short Circuit to GND or PVDD .....Continuous
Duration of Short Circuit Between
OUTP and OUTN..Continuous
Duration of HP_ Short Circuit to GND or V_{DD}...........Continuous
Continuous Power Dissipation (T_A = +70°C)
20-Bump WLP Multilayer Board
(derate 13mW/°C above +70°C)................................1040mW
Junction Temperature ....+150°C
Operating Temperature Range .... -40°C to +85°C
Storage Temperature Range............................ -65°C to +150°C
Lead Temperature (soldering, 10s) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{VDD} = 1.8V, V_{PVDD} = 3.7V, V_{GND} = 0V. Input signal applied at INA configured single-ended, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB, speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Speaker Amplifier Supply Voltage Range	PVDD	Guaranteed by PSRR test		2.7		5.5	V
Headphone Amplifier Supply Voltage Range	V_{DD}	Guaranteed by PSRR test		1.6		2	V
Quiecsent Supply Current		Low-power headphone mode, T_A = +25°C	I_{VDD}		1.35	1.85	mA
			I_{PVDD}		0.35	0.55	
		HP mode, T_A = +25°C, stereo SE input on INA, INB disabled	I_{VDD}		1.35	1.85	
			I_{PVDD}		0.75	1.15	
		SPK mode, T_A = +25°C mono differential Input on INB, INA disabled	I_{VDD}		0.32	0.6	
			I_{PVDD}		1.38	2.2	
		SPK + HP mode, T_A = +25°C, stereo SE input on INA, INB disabled	I_{VDD}		1.35	1.85	
			I_{PVDD}		1.8	2.7	
Shutdown Current	I_{SHDN}	T_A = +25°C, $V_{\overline{SHDN}}$ = 0V	I_{VDD} + I_{PVDD}		0	8	µA
			V_{VDD} = 0V, I_{PVDD}		< 1		
Turn-On Time	t_{ON}	Time from power-on to full operation, including soft-start			10		ms
Input Resistance	R_{IN}	T_A = +25°C, internal gain	Gain = -6dB, -3dB		41.2		kΩ
			Gain = 0dB, 3dB, 6dB, dB	16	20.6	27	
			Gain = 18dB	5.5	7.2	9.6	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VDD} = 1.8V, V_{PVDD} = 3.7V, V_{GND} = 0V. Input signal applied at INA configured single-ended, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB, speaker loads (ZSPK) connected between OUTP and OUTN. Headphone loads (RHP) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V. ZSPK = ∞, RHP = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Resistance	R_F	T_A = +25°C, external gain		19	20	21	kΩ
Maximum Input Signal Swing		Preamp = 0dB			2.3		V_{P-P}
		Preamp = +18dB			0.29		
		Preamp = external gain			2.3 x RINEX/RF		
Common-Mode Rejection Ratio	CMRR	f = 1kHz (differential input mode), gain = 0dB			55		dB
		f = 1kHz (differential input mode), gain = 18dB			32		
Input DC Voltage		IN__ inputs		1.125	1.2	1.275	V
Bias Voltage	V_{BIAS}			1.13	1.2	1.27	V
SPEAKER AMPLIFIER							
Output Offset Voltage	V_{OS}	T_A = +25°C, SPKM = 1			±0.5	±4	mV
		T_A = +25°C, SPKMIX = 0x01, IN_DIFF = 0			±1.5		
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second, volume at mute (Note 2)	Into shutdown		-70		dBV
			Out of shutdown		-70		
Power-Supply Rejection Ratio (Note 2)	PSRR	T_A = +25°C	V_{PVDD} = 2.7V to 5.5V	50	77		dB
			f = 217Hz, 200mV_{P-P} ripple		73		
			f = 1kHz, 200mV_{P-P} ripple		73		
			f = 20kHz, 200mV_{P-P} ripple		57		
Output Power (Note 3)		THD+N ≤ 1%, f = 1kHz, Z_{SPK} = 8Ω + 68µH	V_{PVDD} = 4.2V		920		mW
			V_{PVDD} = 3.7V		700		
			V_{PVDD} = 3.3V		550		
Total Harmonic Distortion Plus Noise	THD+N	f = 1kHz, P_{OUT} = 360mW, T_A = +25°C, R_{SPK} = 8Ω			0.05	0.6	%
Signal-to-Noise Ratio	SNR	A-weighted, SPKMIX = 0x03, referenced to 700mW	IN_DIFF = 0 (single-ended)		96		dB
			IN_DIFF = 1 (differential)		96		

ELECTRICAL CHARACTERISTICS (continued)

(V_{VDD} = 1.8V, V_{PVDD} = 3.7V, V_{GND} = 0V. Input signal applied at INA configured single-ended, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB, speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator Frequency	f_{OSC}				250		kHz
Spread-Spectrum Bandwidth					±20		kHz
Gain				11.5	12	12.5	dB
Current Limit					1.5		A
Efficiency	η	P_{OUT} = 600mW, f = 1kHz			87		%
Output Noise		A-weighted, (SPKMIX = 0x01), IN_DIFF = 1, SPKVOL = -30dB			37		μV_{RMS}
CHARGE PUMP							
Charge-Pump Frequency		V_{HPL} = V_{HPR} = 0V, T_A = +25°C		80	83	85	kHz
		V_{HPL} = V_{HPR} = 0.2V			665		
		V_{HPL} = V_{HPR} = 0.5V			500		
Positive Output Voltage	V_{HPVDD}	V_{HPL}, V_{HPR} > V_{TH}			V_{DD}		V
		V_{HPL}, V_{HPR} < V_{TH}			V_{DD}/2		
Negative Output Voltage	V_{HPVSS}	V_{HPL}, V_{HPR} > V_{TH}			$-V_{DD}$		V
		V_{HPL}, V_{HPR} < V_{TH}			$-V_{DD}$/2		
Headphone Output Voltage Threshold	V_{TH1}	Output voltage at which the charge pump switches between fast and slow clock		$\pm V_{DD}$ x 0.05	$\pm V_{DD}$ x 0.08	$\pm V_{DD}$ x 0.13	V
	V_{TH2}	Output voltage at which the charge pump switches modes, VOUT rising or falling		$\pm V_{DD}$ x 0.21	$\pm V_{DD}$ x 0.25	$\pm V_{DD}$ x 0.3	
Mode Transition Timeouts		Time it takes for the charge pump to transition from Invert to split mode			32		ms
		Time it takes for the charge pump to transition from split to invert mode			20		µs
HEADPHONE AMPLIFIERS							
Output Offset Voltage	V_{OS}	T_A = +25°C, volume at mute			±0.15	±0.6	mV
		T_A = +25°C, HP_MIX = 0x1, IN_DIFF = 0			±0.5		
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second, volume at mute (Note 2)	Into shutdown		-74		dBV
			Out of shutdown		-74		

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

ELECTRICAL CHARACTERISTICS (continued)

(V_{VDD} = 1.8V, V_{PVDD} = 3.7V, V_{GND} = 0V. Input signal applied at INA configured single-ended, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB, speaker loads (ZSPK) connected between OUTP and OUTN. Headphone loads (RHP) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V. ZSPK = ∞, RHP = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio (Note 2)	PSRR	T_A = +25°C	V_{DD} = 1.62V to 1.98V	70	85		dB
			f = 217Hz, V_{RIPPLE} = 200mV_{P-P}		84		
			f = 1kHz, V_{RIPPLE} = 200mV_{P-P}		80		
			f = 20kHz, V_{RIPPLE} = 200mV_{P-P}		69		
Output Power	P_{OUT}	THD+N = 1%, f = 1kHz	R_{HP} = 16Ω		37		mW
			R_{HP} = 32Ω		30		
Channel-to-Channel Gain Tracking		T_A = +25°C, HPL to HPR, HPLMIX = 0x01, HPRMIX = 0x02, IN_DIFF = 0			±0.3	±2.5	%
Total Harmonic Distortion Plus Noise	THD+N	P_{OUT} = 10mW, f = 1kHz	R_{HP} = 32Ω		0.02		%
			R_{HP} = 16Ω		0.03	0.1	
Signal-to-Noise Ratio	SNR	A-weighted, R_{HP} = 16Ω, HPLMIX = 0x01, HPRMIX = 0x02, IN_DIFF = 0			100		dB
Slew Rate	SR				0.35		V/µs
Capacitive Drive	C_L				200		pF
Crosstalk		HPL to HPR, HPR to HPL, f = 20Hz to 20kHz			68		dB
ANALOG SWITCH							
On-Resistance	R_{ON}	$I_{NC_}$ = 20mA, $V_{COM_}$ = 0V and PVDD, SWEN = 1	T_A = +25°C		1.6	4	Ω
			T_A = T_{MIN} to T_{MAX}			5.2	
Total Harmonic Distortion Plus Noise	THD+N	$V_{DIFCOM_}$ = 2V_{P-P}, $V_{CMCOM_}$ = PV_{DD}/2, f = 1kHz, SWEN = 1, Z_{SPK} = 8Ω + 68µH	10Ω in series with each switch		0.05		%
			No series resistors		0.3		
Off-Isolation		SWEN = 0, COM1 and COM2 to GND = 50Ω, f = 10kHz, referred to signal applied to OUTP and OUTN			90		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{VDD} = 1.8V, V_{PVDD} = 3.7V, V_{GND} = 0V. Input signal applied at INA configured single-ended, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB, speaker loads (ZSPK) connected between OUTP and OUTN. Headphone loads (RHP) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V. ZSPK = ∞, RHP = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PREAMPLIFIER							
Gain		PGAIN_ = 000		-6.5	-6	-5.5	dB
		PGAIN_ = 001		-3.5	-3	-2.5	
		PGAIN_ = 010		-0.5	0	+0.5	
		PGAIN_ = 011		2.5	3	3.5	
		PGAIN_ = 100		5.5	6	6.5	
		PGAIN_ = 101		8.5	9	9.5	
		PGAIN_ = 110		17.5	18	18.5	
VOLUME CONTROL							
Volume Level		HP_VOL = 0x1F		5.5	6	6.5	dB
		HP_VOL = 0x00		-68	-64	-60	
		SPKVOL = 0x3F		19	20	21	
		SPKVOL = 0x00		-31	-30	-29	
Mute Attenuation		f = 1kHz	Speaker		100		dB
			Headphone		110		
Zero-Crossing Detection Timeout					100		ms
LIMITER							
Attack Time					1		ms
Release Time Constant		THDT1 = 0			1.4		s
		THDT1 = 1			2.8		

DIGITAL I/O CHARACTERISTICS

(V_{PVDD} = 3.7V, V_{GND} = 0V. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SDA, SCL)						
Input Voltage High	V_{IH}		0.75 x V_{DD}			V
Input Voltage Low	V_{IL}				0.35 x V_{DD}	V
Input Hysteresis	V_{HYS}			200		mV
Input Capacitance	C_{IN}			10		pF
Input Leakage Current	I_{IN}	T_A = +25°C			±1.0	µA
DIGITAL OUTPUTS (SDA Open Drain)						
Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

I2C TIMING CHARACTERISTICS

(V_{PVDD} = 3.7V, V_{GND} = 0V. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a REPEATED START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	(Note 4)	20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 4)	20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F	(Note 4)	20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Note 1: 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: Amplifier inputs are AC-coupled to GND.
Note 3: Class D amplifier testing performed with a resistive load in series with an inductor to simulate an actual speaker load.
Note 4: C_B is in pF.

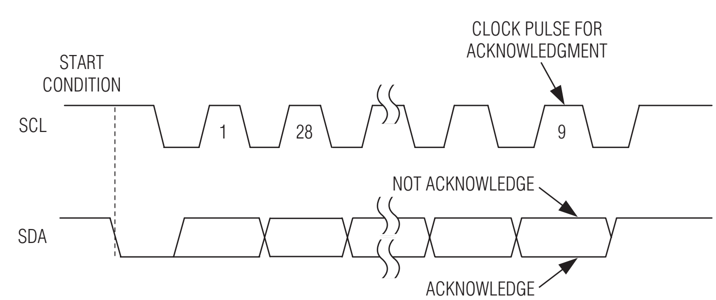
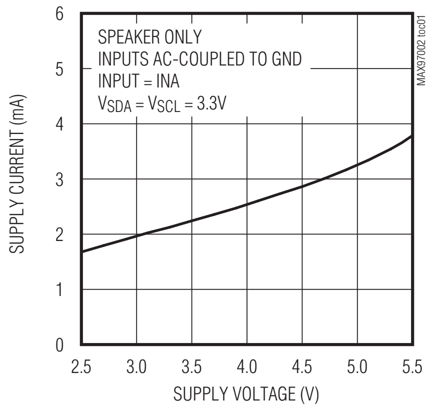


Figure 1. I2C Interface Timing Diagram

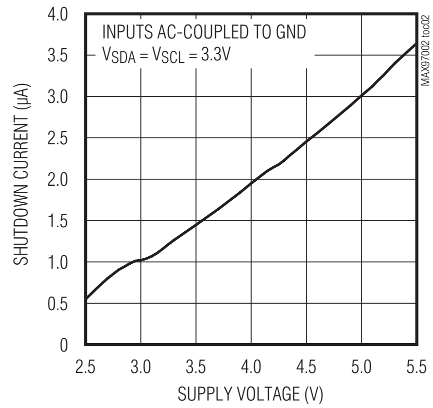
Typical Operating Characteristics

(V_{LDOIN} = V_{PVDD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB. Speaker loads (ZSPK) connected between OUTP and OUTN. Headphone loads (RHP) connected from HPL or HPR to GND. ZSPK = ∞, RHP = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

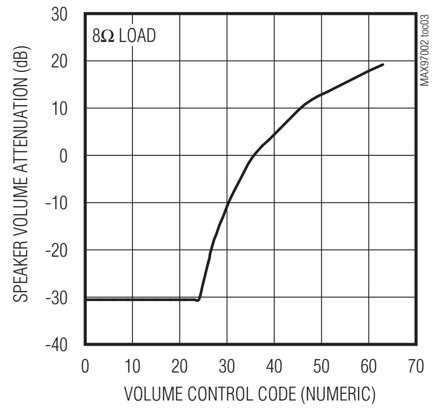
SUPPLY CURRENT vs. SUPPLY VOLTAGE



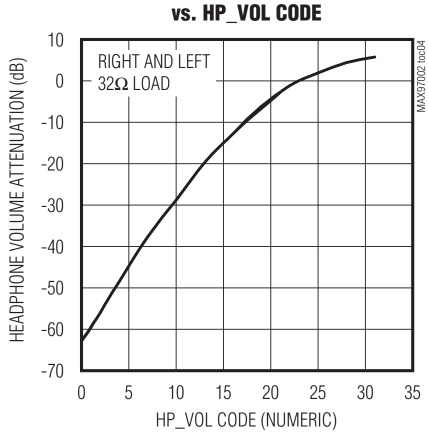
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



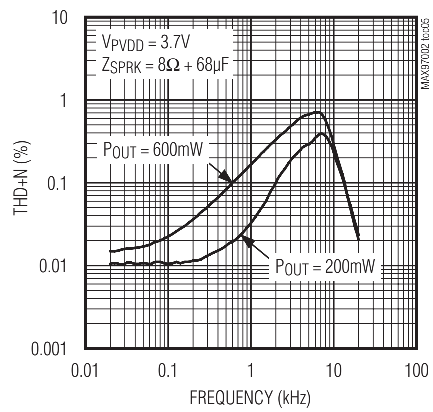
SPEAKER VOLUME ATTENUATION vs. VOLUME CONTROL CODE



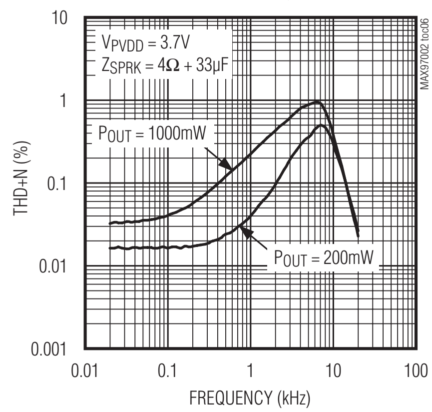
HEADPHONE VOLUME ATTENUATION vs. HP_VOL CODE



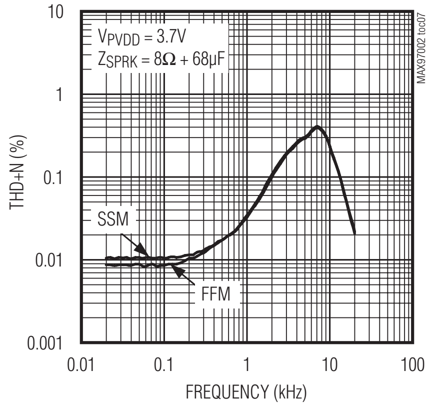
THD+N vs. FREQUENCY



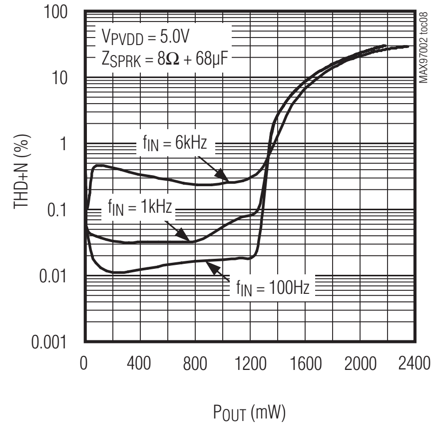
THD+N vs. FREQUENCY



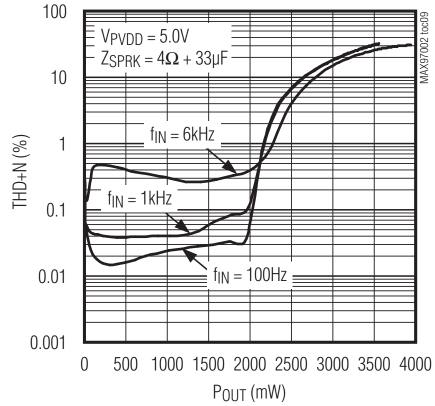
THD+N vs. FREQUENCY



THD+N vs. OUTPUT POWER



THD+N vs. OUTPUT POWER

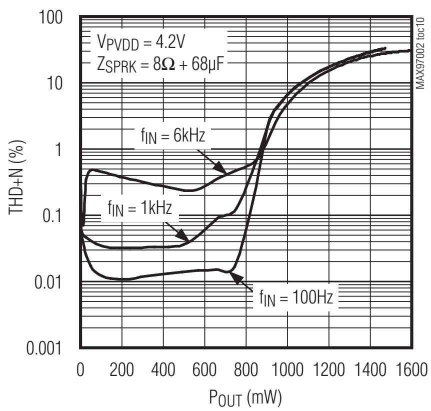


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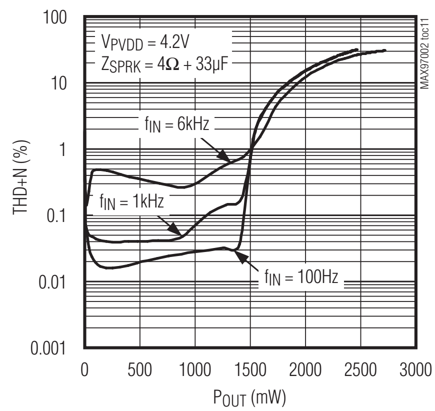
Typical Operating Characteristics (continued)

(V_{LDOIN} = V_{PVDD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB. Speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1μF. T_A = +25°C, unless otherwise noted.)

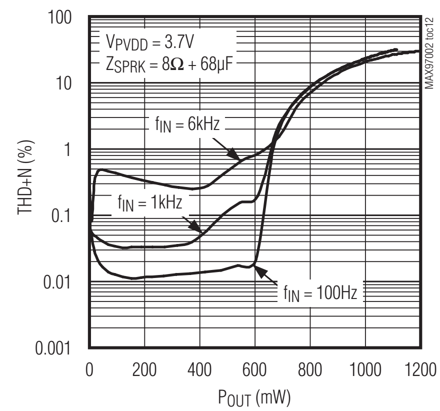
THD+N vs. OUTPUT POWER



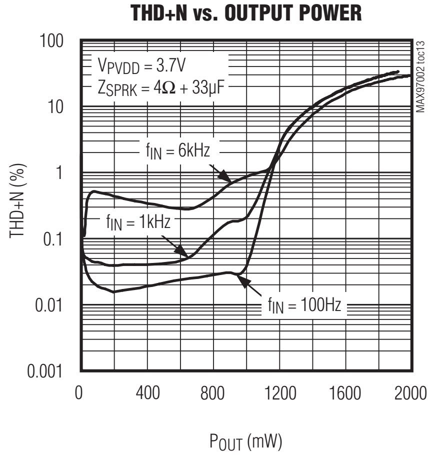
THD+N vs. OUTPUT POWER



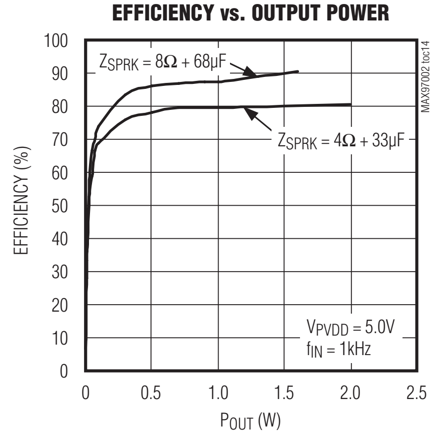
THD+N vs. OUTPUT POWER



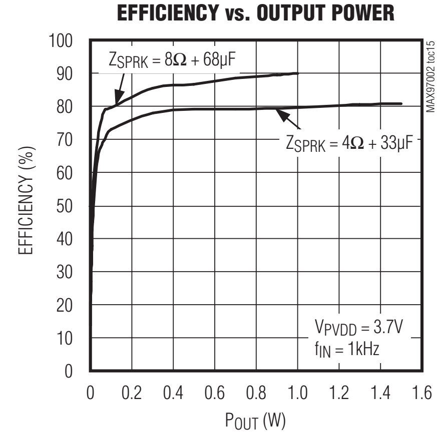
THD+N vs. OUTPUT POWER



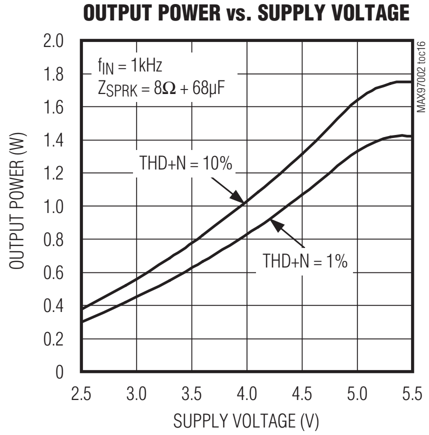
EFFICIENCY vs. OUTPUT POWER



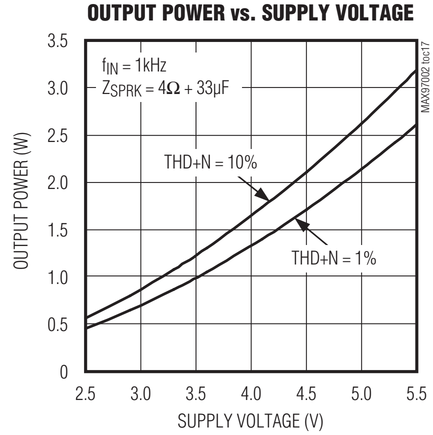
EFFICIENCY vs. OUTPUT POWER



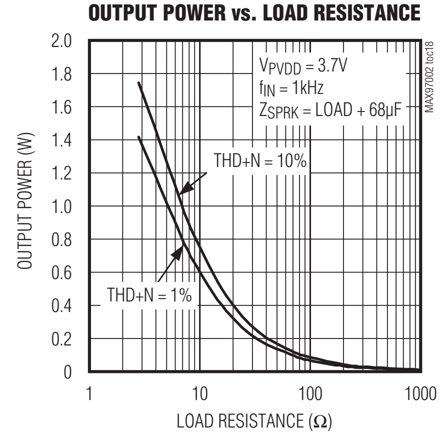
OUTPUT POWER vs. SUPPLY VOLTAGE



OUTPUT POWER vs. SUPPLY VOLTAGE



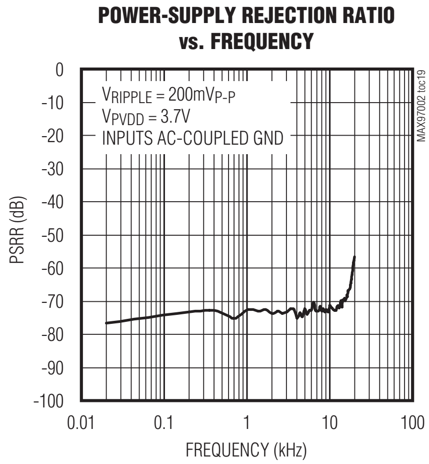
OUTPUT POWER vs. LOAD RESISTANCE

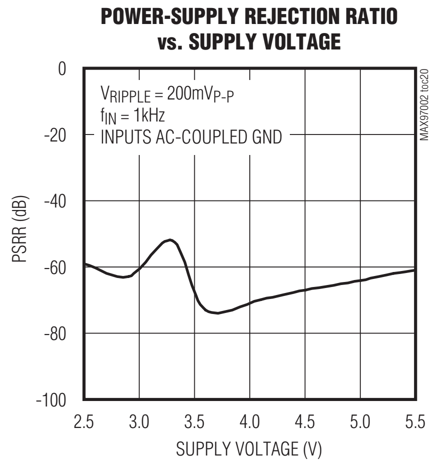


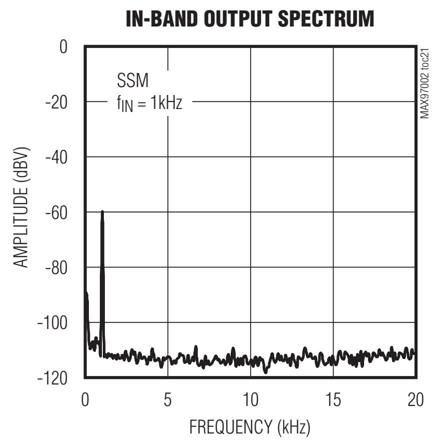
Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

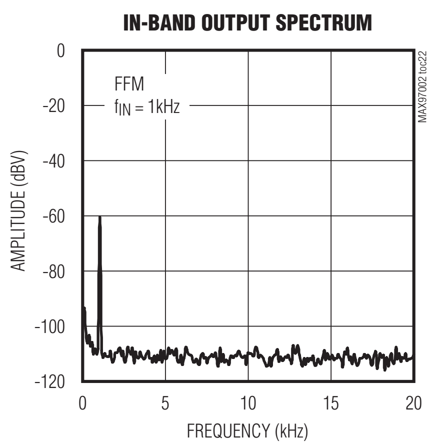
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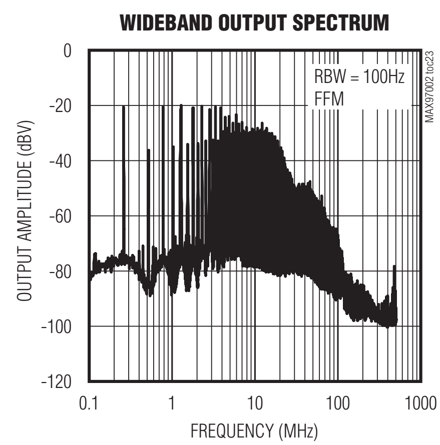
(V_{LDOIN} = V_{PVDD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB. Speaker loads (ZSPK) connected between OUTP and OUTN. Headphone loads (RHP) connected from HPL or HPR to GND. ZSPK = ∞, RHP = ∞. $C_{C1P\text{-}C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1μF. T_A = +25°C, unless otherwise noted.)

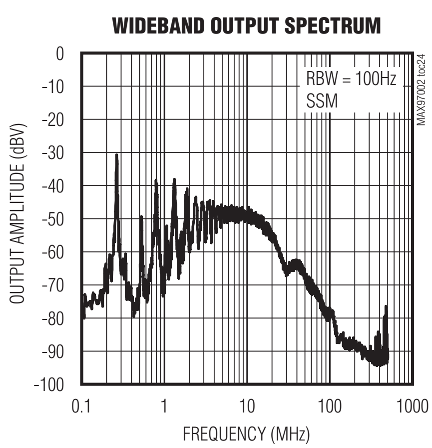


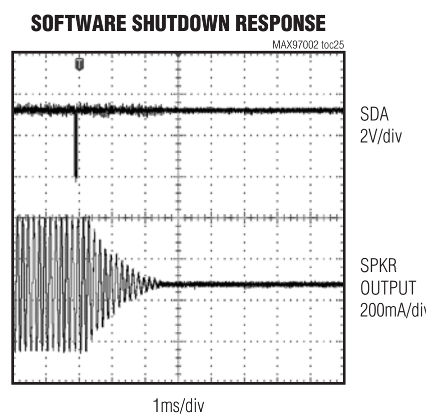










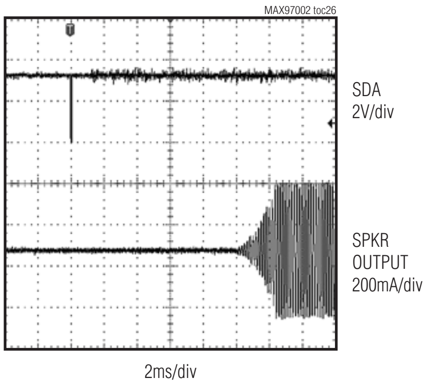


Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

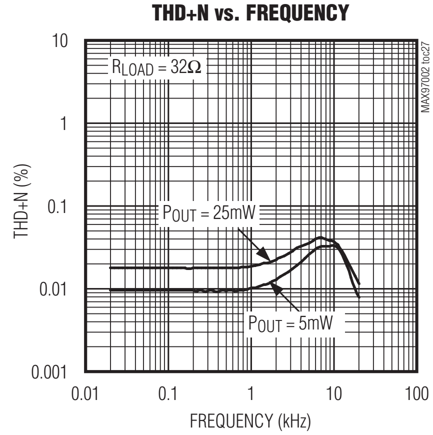
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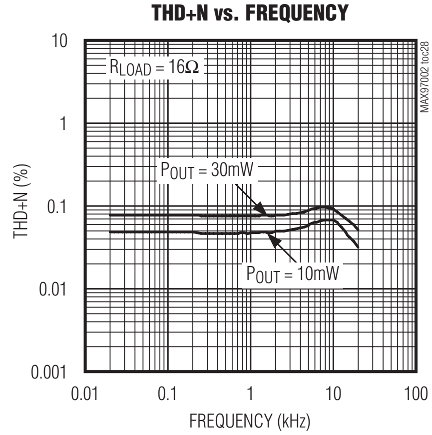
SOFTWARE TURN-ON RESPONSE



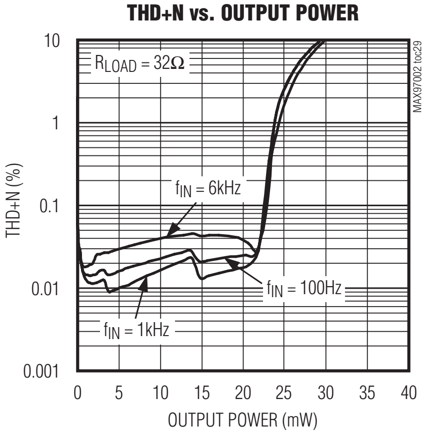
THD+N vs. FREQUENCY



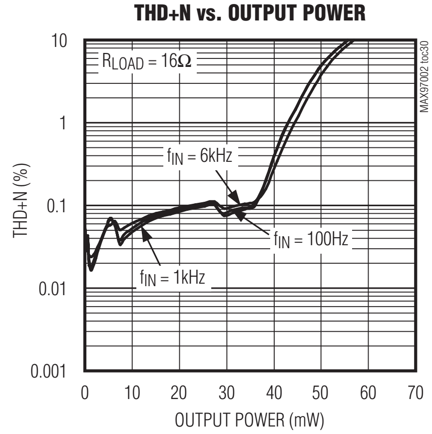
THD+N vs. FREQUENCY



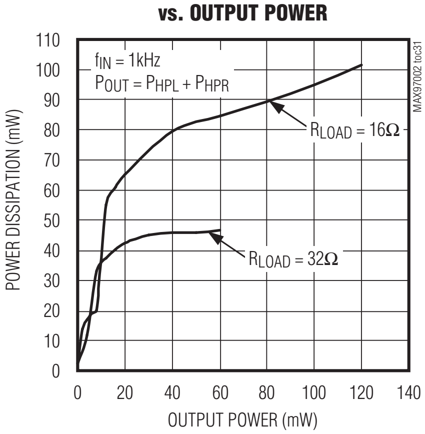
THD+N vs. OUTPUT POWER



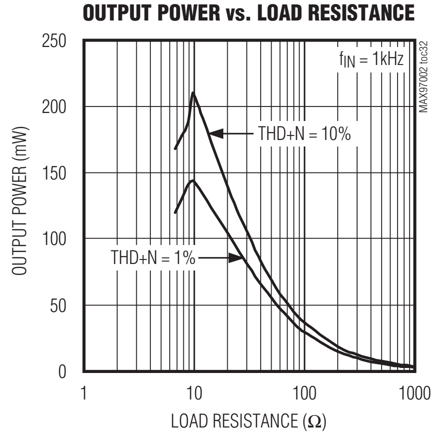
THD+N vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



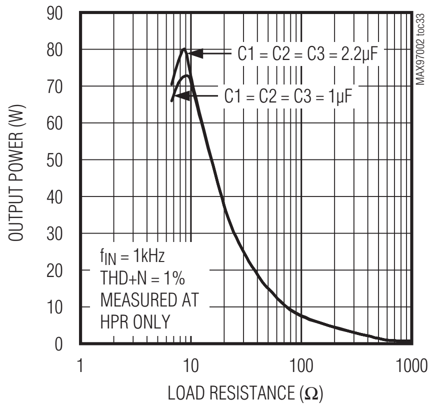
OUTPUT POWER vs. LOAD RESISTANCE



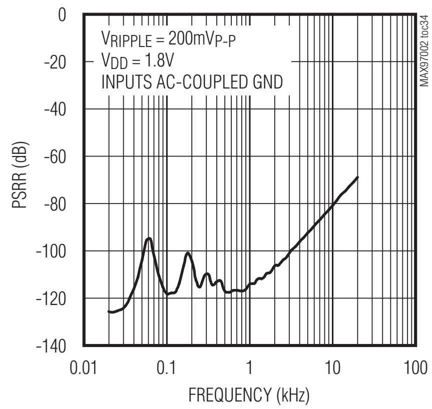
Typical Operating Characteristics (continued)

(V_{LDOIN} = V_{PVDD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB. Speaker loads (ZSPK) connected between OUTP and OUTN. Headphone loads (RHP) connected from HPL or HPR to GND. ZSPK = ∞, RHP = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

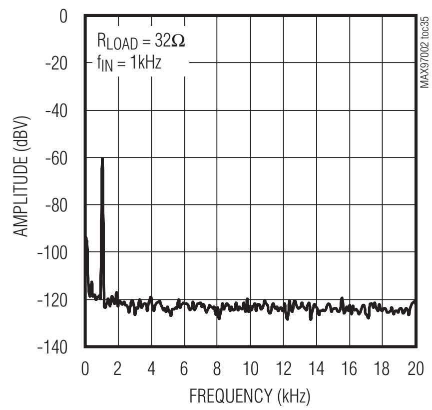
OUTPUT POWER vs. LOAD RESISTANCE



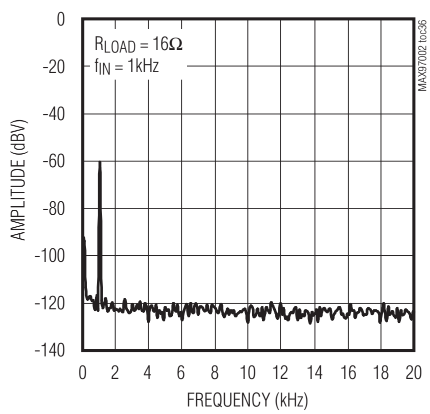
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



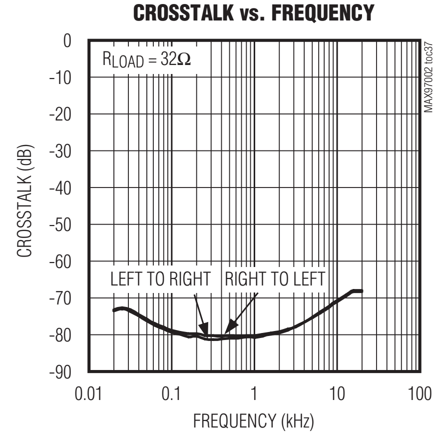
OUTPUT SPECTRUM



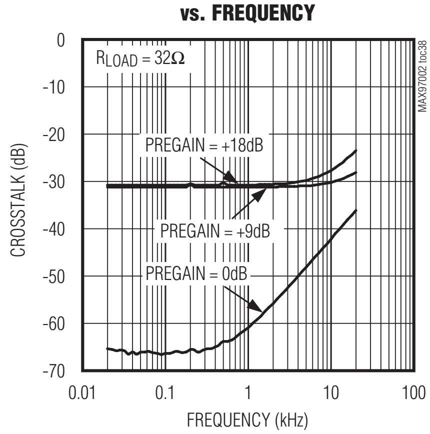
OUTPUT SPECTRUM



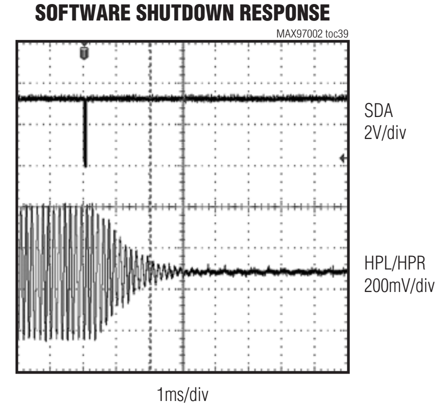
CROSSTALK vs. FREQUENCY



COMMON-MODE REJECTION RATIO vs. FREQUENCY



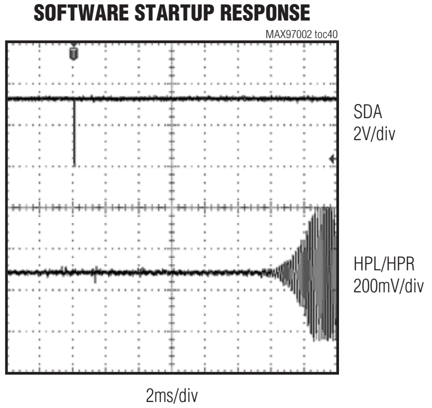
SOFTWARE SHUTDOWN RESPONSE

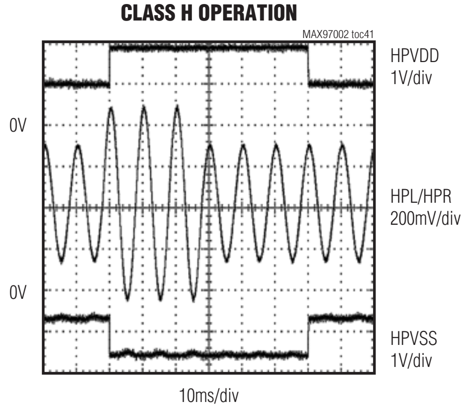


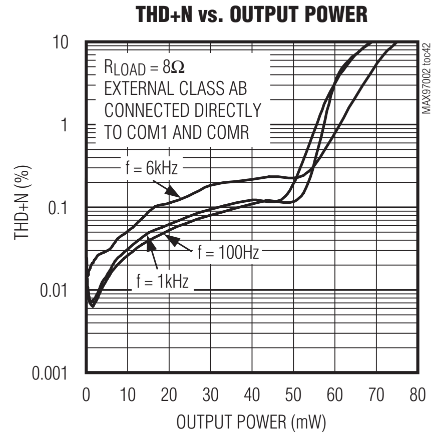
Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

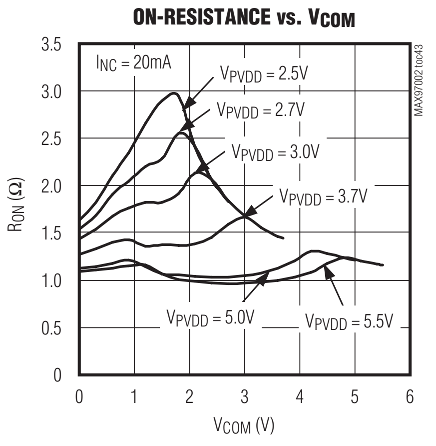
Typical Operating Characteristics (continued)

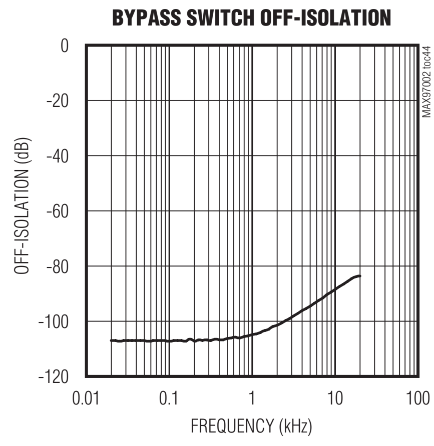
(V_{LDOIN} = V_{PVDD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB. Speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)



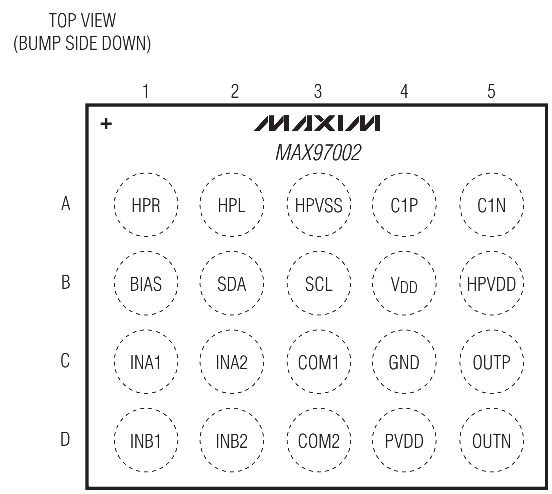








Pin Configuration



Pin Description

PIN	NAME	DESCRIPTION
A1	HPR	Headphone Amplifier Left Output
A2	HPL	Headphone Amplifier Right Output
A3	HPVSS	Headphone Amplifier Negative Power Supply. Bypass with a 1µF capacitor to GND.
A4	C1P	Charge-Pump Flying Capacitor Positive Terminal. Connect a 1µF capacitor between C1P and C1N.
A5	C1N	Charge-Pump Flying Capacitor Negative Terminal. Connect a 1µF capacitor between C1P and C1N.
B1	BIAS	Common-Mode Bias. Bypass to GND with a 1µF capacitor.
B2	SDA	Serial-Data Input/Output. Connect a pullup resistor from SDA to DVDD.
B3	SCL	Serial-Clock Input. Connect a pullup resistor from SCL to DVDD.
B4	V_{DD}	Headphone Amplifier Supply. Bypass with a 1µF capacitor to GND.
B5	HPVDD	Headphone Amplifier Positive Power Supply. Bypass with a 1µF capacitor to GND.
C1	INA1	Input A1. Left input or negative input.
C2	INA2	Input A2. Right input or positive input.
C3	COM1	Positive Bypass Switch Input
C4	GND	Analog Ground
C5	OUTP	Positive Speaker Output
D1	INB1	Input B1. Left input or negative input.
D2	INB2	Input B2. Right input or positive input.
D3	COM2	Negative Bypass Switch Input
D4	PVDD	Class D Power Supply. Bypass with a 1µF capacitor to GND.
D5	OUTN	Negative Speaker Output

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

Detailed Description

The MAX97002 mono audio subsystem combines a mono speaker amplifier with a stereo headphone amplifier and an analog DPST switch. The high-efficiency 700mW Class D speaker amplifier operates directly from the battery and consumes no more than 1µA when in shutdown mode. The headphone amplifier utilizes a dual-mode charge pump and a Class H output stage to maximize efficiency while outputting a ground-referenced signal that does not require output coupling capacitors. The headphone and speaker amplifiers have independent volume control and on/off control. The 4 inputs are configurable as 2 differential inputs or 4 single-ended inputs. All control is performed using the 2-wire I²C interface.

The speaker amplifier incorporates a distortion limiter to automatically reduce the volume level when excessive clipping occurs. This allows high gain for low-level signals without compromising the quality of large signals.

Signal Path

The MAX97002 signal path consists of flexible inputs, signal mixing, volume control, and output amplifiers (Figure 2). The inputs can be configured for single-ended or differential signals (Figure 3). The internal preamplifiers feature programmable gain settings using internal resistors and an external gain setting using a trimmed internal feedback resistor. The external option allows any desired gain to be selected. Following preamplification, the input signals are mixed, volume adjusted, and routed to the headphone and speaker amplifiers based on the desired configuration.

Mixers

The MAX97002 features independent mixers for the left headphone, right headphone, and speaker paths. Each output can select any combination of any inputs. This allows for mixing two audio signals together and routing independent signals to the headphone and speaker amplifiers. If one of the inputs is not selected by either mixer, it is automatically powered down to save power.

Class D Speaker Amplifier

The MAX97002 Class D speaker amplifier utilizes active emissions limiting and spread-spectrum modulation to minimize the EMI radiated by the amplifier.

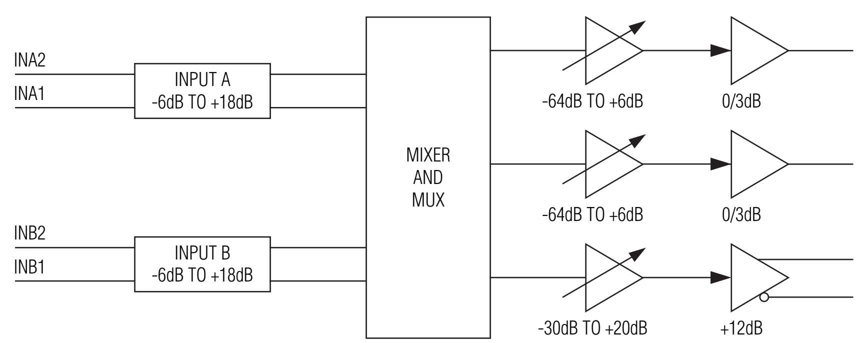


Figure 2. Signal Path

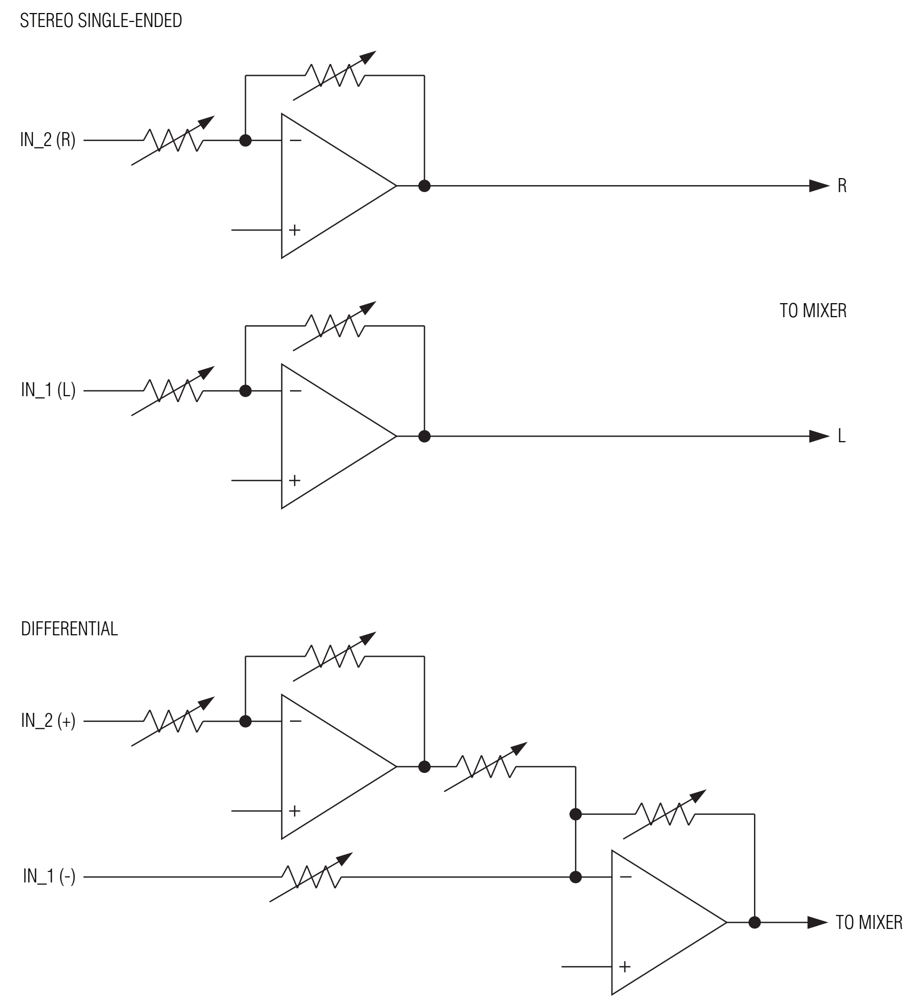


Figure 3. Differential and Stereo Single-Ended Input Configurations

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

Ultra-Low EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters or shielding in order to meet EN55022B electromagnetic-interference (EMI) regulation standards. Maxim's active emissions limiting edge-rate control circuitry and spread-spectrum modulation reduces EMI emissions, while maintaining up to 87% efficiency. Maxim's spread-spectrum modulation mode flattens wideband spectral components, while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The MAX97002's spread-spectrum modulator randomly varies the switching frequency by ±20kHz around the center frequency (250kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes (see Figure 4).

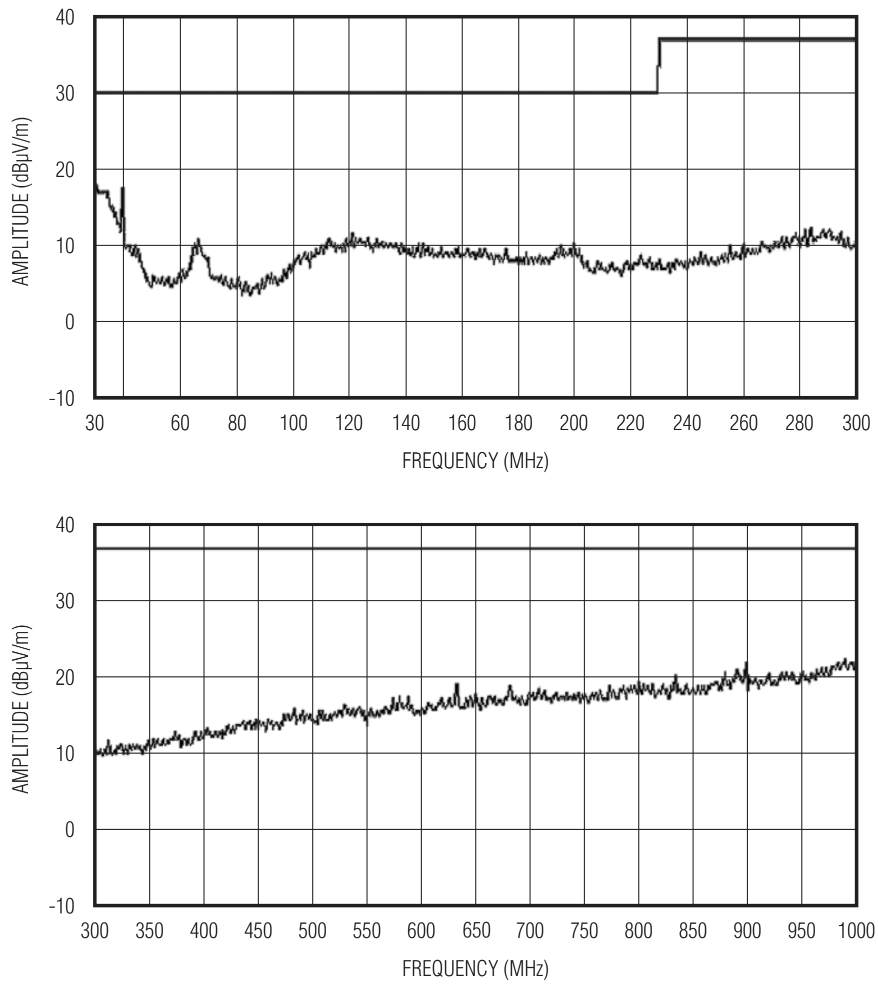


Figure 4. EMI with 15cm of Speaker Cable

Distortion Limiter

The MAX97002 speaker amplifiers integrate a limiter to provide speaker protection and audio compression. When enabled, the limiter monitors the audio signal at the output of the Class D speaker amplifier and decreases the gain if the distortion exceeds the predefined threshold. The limiter automatically tracks the battery voltage to reduce the gain as the battery voltage drops.

Figure 5 shows the typical output vs. input curves with and without the distortion limiter. The dotted line shows the maximum gain for a given distortion limit without the distortion limiter. The solid line shows how, with the distortion limiter enabled, the gain can be increased without exceeding the set distortion limit. When the limiter is enabled, selecting a high gain level results in peak signals being attenuated while low signals are left unchanged. This increases the perceived loudness without the harshness of a clipped waveform.

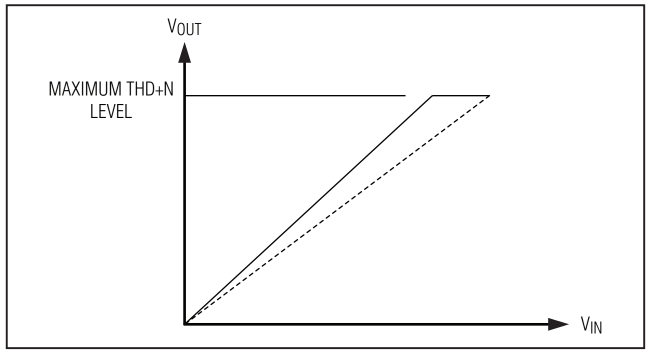


Figure 5. Limiter Gain Curve

Analog Switch

The MAX97002 integrates a DPST analog audio switch that connects COM1 and COM2 to OUTP and OUTN, respectively. Unlike discrete solutions, the switch design reduces coupling of Class D switching noise to the COM_ inputs. This eliminates the need for a costly T-switch. Drive COM1 and COM2 with a low-impedance source to minimize noise on the pins. In applications that do not require the analog switch, leave COM1 and COM2 unconnected. When applying signal on COM1 and COM2, disable the Class D amplifier before closing the switch.

Headphone Amplifier

DirectDrive

Traditional single-supply headphone amplifiers have outputs biased at a nominal DC voltage (typically half the supply). Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier.

Maxim's DirectDrive® architecture uses a charge pump to create an internal negative supply voltage. This allows the headphone outputs of the MAX97002 to be biased at GND while operating from a single supply (Figure 6). Without a DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220µF, typ) capacitors, the MAX97002 charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. See the Output Power vs. Load Resistance graph in the *Typical Operating Characteristics* for details of the possible capacitor sizes. There is a low DC voltage on the amplifier outputs due to amplifier offset. However, the offset of the MAX97002 is typically ±0.6mV, which, when combined with a 32Ω load, results in less than 50µA of DC current flow to the headphones.

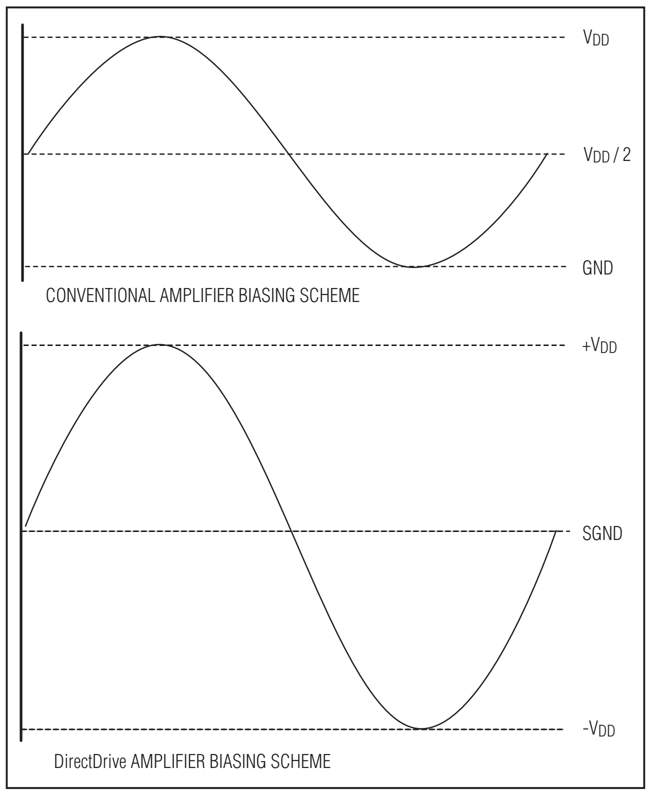


Figure 6.Traditional Amplifier Output vs. MAX97002 DirectDrive Output

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

In addition to the cost and size disadvantages of the DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal. Previous attempts at eliminating the output-coupling capacitors involved biasing the headphone return (sleeve) to the DC-bias voltage of the headphone amplifiers. This method raises some issues:

- The sleeve is typically grounded to the chassis. Using the midrail biasing approach, the sleeve must be isolated from system ground, complicating product design.
- During an ESD strike, the amplifier's ESD structures are the only path to system ground. Thus, the amplifier must be able to withstand the full energy from an ESD strike.
- When using the headphone jack as a line out to other equipment, the bias voltage on the sleeve may conflict with the ground potential from other equipment, resulting in possible damage to the amplifiers.

Charge Pump

The MAX97002's dual-mode charge pump generates both the positive and negative power supply for the headphone amplifier. To maximize effficiency, both the charge pump's switching frequency and output voltage change based on signal level.

When the input signal level is less than 10% of V_{DD} the switching frequency is reduced to a low rate. This minimizes switching losses in the charge pump. When the input signal exceeds 10% of V_{DD}, the switching frequency increases to support the load current.

For input signals below 25% of V_{DD}, the charge pump generates $\pm(V_{DD}/2)$ to minimize the voltage drop across the amplifier's power stage and thus improves efficiency. Input signals that exceed 25% of V_{DD} cause the charge pump to output $\pm V_{DD}$. The higher output voltage allows for full output power from the headphone amplifier.

To prevent audible glitches when transitioning from the $\pm(V_{DD}/2)$ output mode to the $\pm V_{DD}$ output mode, the charge pump transitions very quickly. This quick change draws significant current from V_{DD} for the duration of the transition. The bypass capacitor on V_{DD} supplies the required current and prevent droop on V_{DD}.

The charge pump's dynamic switching mode can be turned off through the I²C interface. The charge pump can then be forced to output either $\pm(V_{DD}/2)$ or $\pm V_{DD}$ regardless of input signal level.

Class H Operation

A Class H amplifier uses a Class AB output stage with power supplies that are modulated by the output signal. In the case of the MAX97002, two nominal power-supply differentials of 1.8V (+0.9V to -0.9V) and 3.6V (+1.8V to -1.8V) are available from the charge pump. Figure 7 shows the operation of the output voltage dependent power supply.

Low-Power Mode

To minimize power consumption when using the headphone amplifier, enable the low-power mode. In this mode, the headphone mixers and volume control are bypassed and shutdown.

I²C Slave Address

The MAX97002 uses a slave address of 0x9A or 1001101R/W. The address is defined as the 7 most significant bits (MSBs) followed by the read/write bit. Set the read/write bit to 1 to configure the MAX97002 to read mode. Set the read/write bit to 0 to configure the MAX97002 to write mode. The address is the first byte of information sent to the MAX97002 after the START (S) condition.

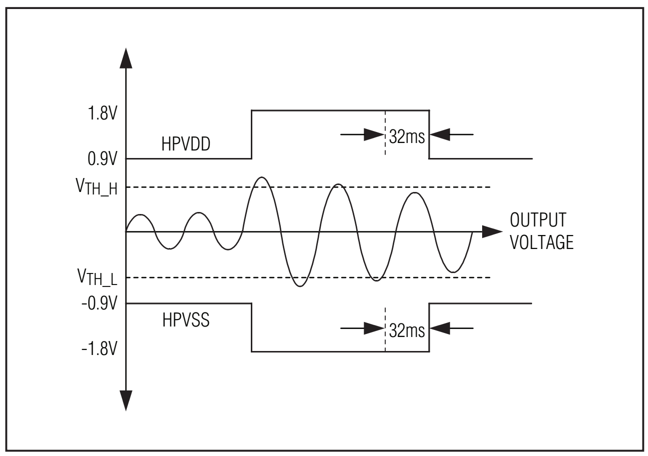


Figure 7. Class H Operation

I²C Registers

Nine internal registers program the MAX97002. Table 1 lists all of the registers, their addresses, and power-on-reset states. Register 0xFF indicates the device revision.

Write zeros to all unused bits in the register table when updating the register, unless otherwise noted. Tables 2–7 describe each bit.

Table 1. Register Map

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W
STATUS											
Input Gain	INADIFF	INBDIFF	PGAINA			PGAINB			0x00	0x00	R/W
Headphone Mixers	HPLMIX				HPRMIX				0x01	0x00	R/W
Speaker Mixer	0	0	0	0	SPKMIX				0x02	0x00	R/W
Headphone Left	$\overline{\text{ZCD}}$	$\overline{\text{SLEW}}$	HPLM	HPLVOL					0x03	0x00	R/W
Headphone Right	HPGAIN	0	HPRM	HPRVOL					0x04	0x00	R/W
Speaker	FFM	SPKM	SPKVOL						0x05	0x00	R/W
Reserved	0	0	0	0	0	0	0	0	0x06	0x00	R/W
Limiter	THDCLP				0	0	0	THDT1	0x07	0x00	R/W
Power Management	$\overline{\text{SHDN}}$	LPMODE		SPKEN	0	HPLEN	HPREN	BYPEN	0x08	0x01	R/W
Charge Pump	0	0	0	0	0	0	CPSEL	FIXED	0x09	0x00	R/W
REVISION ID											
Rev ID	REV								0xFF	0x00	R

Table 2. Input Register

REGISTER	BIT	NAME	DESCRIPTION
0x00	7	INADIFF	**Input A Differential Mode.** Configures the input A channel as either a mono differential signal (INA = INA2 - INA1) or as a stereo signal (INA1 = left, INA2 = right). 0 = Stereo single-ended 1 = Differential
	6	INBDIFF	**Input B Differential Mode.** Configures the input B channel as either a mono differential signal (INB = INB2 - INB1) or as a stereo signal (INB1 = left, INB2 = right). 0 = Stereo single-ended 1 = Differential
	5	PGAINA	**Input A Preamp Gain.** Set the input gain to maximize output signal level for a given input signal range to improve the SNR of the system. PGAINA = 111 switches to a trimmed 20kΩ feedback resistor for external gain setting.
	4		**VALUE** — **LEVEL (dB)** 000 — -6 001 — -3 010 — 0 011 — 3 100 — 6 101 — 9 110 — 18 111 — External
	3		
	2	PGAINB	**Input B Preamp Gain.** Set the input gain to maximize output signal level for a given input signal range to improve the SNR of the system. PGAINB = 111 switches to a trimmed 20kΩ feedback resistor for external gain setting.
	1		**VALUE** — **LEVEL (dB)** 000 — -6 001 — -3 010 — 0 011 — 3 100 — 6 101 — 9 110 — 18 111 — External
	0		

Table 3. Mixer Registers

REGISTER	BIT	NAME	DESCRIPTION
0x01	7	HPLMIX	**Left Headphone Mixer.** Selects which of the four inputs is routed to the left headphone output.
	6		**VALUE** — **INPUT** 0000 — No input xxx1 — INA1 (disabled when INADIFF = 1) xx1x — INA2 (select when INADIFF = 1) x1xx — INB1 (disabled when INBDIFF = 1) 1xxx — INB2 (select when INBDIFF = 1)
	5		
	4		
	3	HPRMIX	**Right Headphone Mixer.** Selects which of the four inputs is routed to the right headphone output.
	2		**VALUE** — **INPUT** 0000 — No input xxx1 — INA1 (disabled when INADIFF = 1) xx1x — INA2 (select when INADIFF = 1) x1xx — INB1 (disabled when INBDIFF = 1) 1xxx — INB2 (select when INBDIFF = 1)
	1		
	0		
0x02	3	SPKMIX	**Speaker Mixer.** Selects which of the four inputs is routed to the speaker output.
	2		**VALUE** — **INPUT** 0000 — No input xxx1 — INA1 (disabled when INADIFF = 1) xx1x — INA2 (select when INADIFF = 1) x1xx — INB1 (disabled when INBDIFF = 1) 1xxx — INB2 (select when INBDIFF = 1)
	1		
	0		

Table 4. Volume Control Registers

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="21">0x03</td><td>7</td><td>$\overline{\text{ZCD}}$</td><td colspan="4">Zero-Crossing Detection. Determines whether zero-crossing detection is used on all volume control changes to reduce clicks and pops. Disabling zero-crossing detection allows volume changes to occur immediately.
0 = Enabled
1 = Disabled</td></tr>
<tr><td>6</td><td>$\overline{\text{SLEW}}$</td><td colspan="4">Volume Slewing. Determines whether volume slewing is used on all volume control changes to reduce clicks and pops. When enabled, volume changes cause the MAX97002 to ramp through intermediate volume settings whenever a change to the volume is made. If $\overline{\text{ZCD}}$ = 1, slewing occurs at a rate of 0.2ms per step. If $\overline{\text{ZCD}}$ = 0, slew time depends on the input signal. Write a 1 to this bit to disable slewing and implement volume changes immediately. This bit also activates soft-start at power-on and soft-stop and power-off.
0 = Enabled
1 = Disabled</td></tr>
<tr><td>5</td><td>HPLM</td><td colspan="4">Left Headphone Mute
0 = Unmuted
1 = Muted</td></tr>
<tr><td rowspan="2">4</td><td rowspan="18">HPLVOL</td><td colspan="4">Left Headphone Volume</td></tr>
<tr><td>VALUE</td><td>LEVEL (dB)</td><td>VALUE</td><td>LEVEL (dB)</td></tr>
<tr><td rowspan="5">3</td><td>0x00</td><td>-64</td><td>0x10</td><td>-12</td></tr>
<tr><td>0x01</td><td>-60dB</td><td>0x11</td><td>-10</td></tr>
<tr><td>0x02</td><td>-56</td><td>0x12</td><td>-8</td></tr>
<tr><td>0x03</td><td>-52</td><td>0x13</td><td>-6</td></tr>
<tr><td>0x04</td><td>-48</td><td>0x14</td><td>-4</td></tr>
<tr><td rowspan="4">2</td><td>0x05</td><td>-44</td><td>0x15</td><td>-2</td></tr>
<tr><td>0x06</td><td>-40</td><td>0x16</td><td>-1</td></tr>
<tr><td>0x07</td><td>-37</td><td>0x17</td><td>0</td></tr>
<tr><td>0x08</td><td>-34</td><td>0x18</td><td>1</td></tr>
<tr><td rowspan="6">1</td><td>0x09</td><td>-31</td><td>0x19</td><td>2</td></tr>
<tr><td>0x0A</td><td>-28</td><td>0x1A</td><td>3</td></tr>
<tr><td>0x0B</td><td>-25</td><td>0x1B</td><td>4</td></tr>
<tr><td>0x0C</td><td>-22</td><td>0x1C</td><td>4.5</td></tr>
<tr><td>0x0D</td><td>-19</td><td>0x1D</td><td>5</td></tr>
<tr><td>0x0E</td><td>-16</td><td>0x1E</td><td>5.5</td></tr>
<tr><td>0</td><td>0x0F</td><td>-14</td><td>0x1F</td><td>6</td></tr>
</table>

Table 4. Volume Control Registers (continued)

REGISTER	BIT	NAME	DESCRIPTION			
0x04	7	HPGAIN	**Headphone Gain.** Controls the headphone amplifier gain. 0 = 0dB 1 = 3dB			
	5	HPRM	**Right Headphone Mute** 0 = Unmuted 1 = Muted			
	4	HPRVOL	**Right Headphone Volume**			
			VALUE	**LEVEL (dB)**	**VALUE**	**LEVEL (dB)**
	3		0x00	-64	0x10	-12
			0x01	-60dB	0x11	-10
			0x02	-56	0x12	-8
			0x03	-52	0x13	-6
	2		0x04	-48	0x14	-4
			0x05	-44	0x15	-2
			0x06	-40	0x16	-1
			0x07	-37	0x17	0
	1		0x08	-34	0x18	1
			0x09	-31	0x19	2
			0x0A	-28	0x1A	3
			0x0B	-25	0x1B	4
			0x0C	-22	0x1C	4.5
	0		0x0D	-19	0x1D	5
			0x0E	-16	0x1E	5.5
			0x0F	-14	0x1F	6

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

Table 4. Volume Control Registers (continued)

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="6">DESCRIPTION</th></tr>
<tr><td rowspan="18">0x05</td><td>7</td><td>FFM</td><td colspan="6">Fixed-Frequency Oscillation. Removes spread spectrum from the Class D oscillator.
0 = Spread-spectrum mode
1 = Fixed-frequency mode</td></tr>
<tr><td>6</td><td>SPKM</td><td colspan="6">Speaker Mute
0 = Unmuted
1 = Mute</td></tr>
<tr><td rowspan="2">5</td><td rowspan="16">SPKVOL</td><td colspan="6">Speaker Volume</td></tr>
<tr><th>VALUE</th><th>LEVEL (dB)</th><th>VALUE</th><th>LEVEL (dB)</th><th>VALUE</th><th>LEVEL (dB)</th></tr>
<tr><td rowspan="4">4</td><td>0x00–0x18</td><td>-30</td><td>0x26</td><td>3</td><td>0x34</td><td>14.5</td></tr>
<tr><td>0x19</td><td>-26</td><td>0x27</td><td>4</td><td>0x35</td><td>15</td></tr>
<tr><td>0x1A</td><td>-22</td><td>0x28</td><td>5</td><td>0x36</td><td>15.5</td></tr>
<tr><td>0x1B</td><td>-18</td><td>0x29</td><td>6</td><td>0x37</td><td>16</td></tr>
<tr><td rowspan="3">3</td><td>0x1C</td><td>-14</td><td>0x2A</td><td>7</td><td>0x38</td><td>16.5</td></tr>
<tr><td>0x1D</td><td>-12</td><td>0x2B</td><td>8</td><td>0x39</td><td>17</td></tr>
<tr><td>0x1E</td><td>-10</td><td>0x2C</td><td>9</td><td>0x3A</td><td>17.5</td></tr>
<tr><td rowspan="3">2</td><td>0x1F</td><td>-8</td><td>0x2D</td><td>10</td><td>0x3B</td><td>18</td></tr>
<tr><td>0x20</td><td>-6</td><td>0x2E</td><td>11</td><td>0x3C</td><td>18.5</td></tr>
<tr><td>0x21</td><td>-4</td><td>0x2F</td><td>12</td><td>0x3D</td><td>19</td></tr>
<tr><td rowspan="3">1</td><td>0x22</td><td>-2</td><td>0x30</td><td>12.5</td><td>0x3E</td><td>19.5</td></tr>
<tr><td>0x23</td><td>0</td><td>0x31</td><td>13</td><td>0x3F</td><td>20</td></tr>
<tr><td>0x24</td><td>1</td><td>0x32</td><td>13.5</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td>0</td><td>0x25</td><td>2</td><td>0x33</td><td>14</td></tr>
</table>

Distortion Limiter

Table 5. Distortion Limiter Register

REGISTER	BIT	NAME	DESCRIPTION	
0x07	7	THDCLP	**Distortion Limit**	
			VALUE	**THD LIMIT (%)**
	6		0000	Disabled
			0001–1001	≤ 4
			1010	≤ 5
	5		1011	≤ 6
			1100	≤ 8
			1101	≤ 11
	4		1110	≤ 12
			1111	≤ 15
			0000	Disabled
	0	THDT1	**Distortion Release Time Constant** 0 = 1.4s 1 = 2.8s	

Power Management

Table 6. Power Management Register

REGISTER	BIT	NAME	DESCRIPTION	
0x08	7	$\overline{\text{SHDN}}$	**Software Shutdown** 0 = Device disabled 1 = Device enabled	
	6	LPMODE	**Low-Power Headphone Mode.** Enables low-power headphone mode. When activated this mode directly connects the selected channel to the headphone amplifiers, bypassing the mixers and the volume control. Additionally, low-power mode disables the speaker path.	
			VALUE	**LIMIT**
	5		00	Disabled
			01	INA (SE) Connected to the headphone output
			10	INB (SE) Connected to the headphone output
			11	INA (Diff) to HPL and INB (Diff) to HPR
	4	SPKEN	**Speaker Amplifier Enable** 0 = Disabled 1 = Enabled	
	2	HPLEN	**Left Headphone Amplifier Enable** 0 = Disabled 1 = Enabled	
	1	HPREN	**Right Headphone Amplifier Enable** 0 = Disabled 1 = Enabled	
	0	BYPEN	**Analog Switch** 0 = Open 1 = Closed	

Charge-Pump Control

Table 7. Charge-Pump Control Register

REGISTER	BIT	NAME	DESCRIPTION
0x09	1	CPSEL	**Charge-Pump Output Select.** Works with the FIXED to set ±1.8V or ±0.9V outputs on HPVDD and HPVSS. Ignored when FIXED = 0. 0 = ±1.8V on HPVDD/HPVSS 1 = ±0.9V on HPVDD/HPVSS
	0	FIXED	**Class H Mode.** When enabled, this bit forces the charge pump to generate static power rails for HPVDD and HPVSS, instead of dynamically adjusting them based on output signal level. 0 = Class H mode 1 = Fixed-supply mode

I²C Serial Interface

The MAX97002 features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX97002 and the master at clock rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX97002 by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX97002 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX97002 transmits the proper slave address followed by a series of nine SCL pulses. The MAX97002 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX97002 from high voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 8). A START condition from the master signals the beginning of a transmission to the MAX97002. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

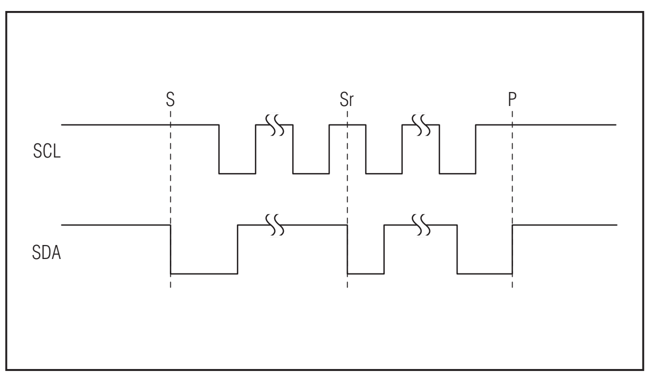


Figure 8. START, STOP, and REPEATED START Conditions

SMBus is a trademark of Intel Corp.

Early STOP Conditions

The MAX97002 recognizes a STOP (P) condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START (S) condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For the MAX97002 the 7 MSBs are 1001101. Setting the read/write bit to 1 (slave address = 0x9B) configures the MAX97002 for read mode. Setting the read/write bit to 0 (slave address = 0x9A) configures the MAX97002 for write mode. The address is the first byte of information sent to the MAX97002 after the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX97002 uses to handshake receipt each byte of data when in write mode (Figure 9). The MAX97002 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX97002 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX97002, followed by a STOP condition.

Write Data Format

A write to the MAX97002 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 10 illustrates the proper frame format for writing one byte of data to the MAX97002. Figure 11 illustrates the frame format for writing n-bytes of data to the MAX97002.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX97002. The MAX97002 acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the MAX97002's internal register address pointer. The pointer tells the MAX97002 where to write the next byte of data. An acknowledge pulse is sent by the MAX97002 upon receipt of the address pointer data.

The third byte sent to the MAX97002 contains the data that is written to the chosen register. An acknowledge pulse from the MAX97002 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. Register addresses greater than 0x09 are reserved. Do not write to these addresses.

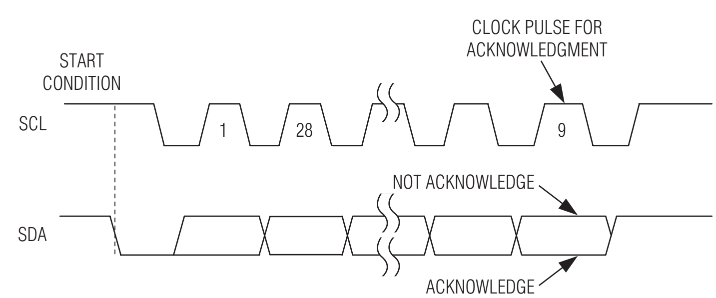


Figure 9. Acknowledge

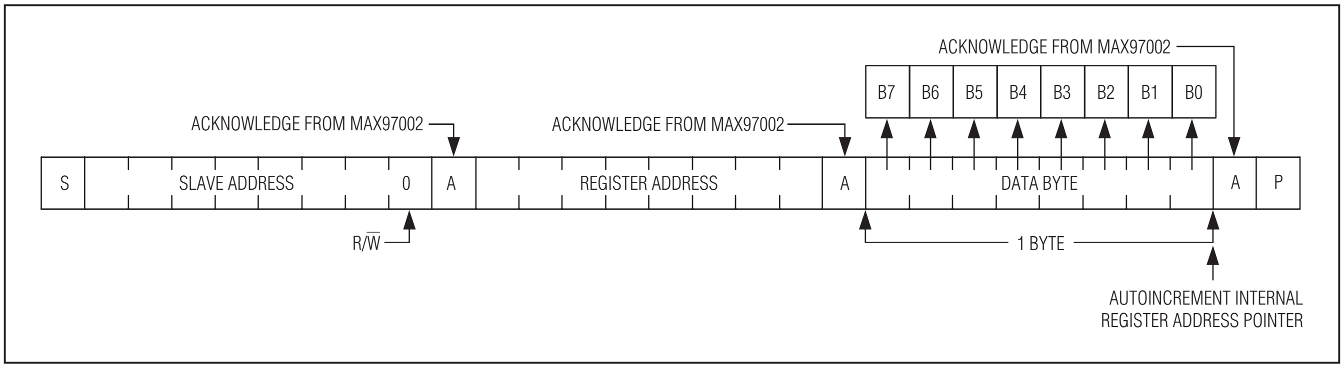


Figure 10. Writing One Byte of Data to the MAX97002

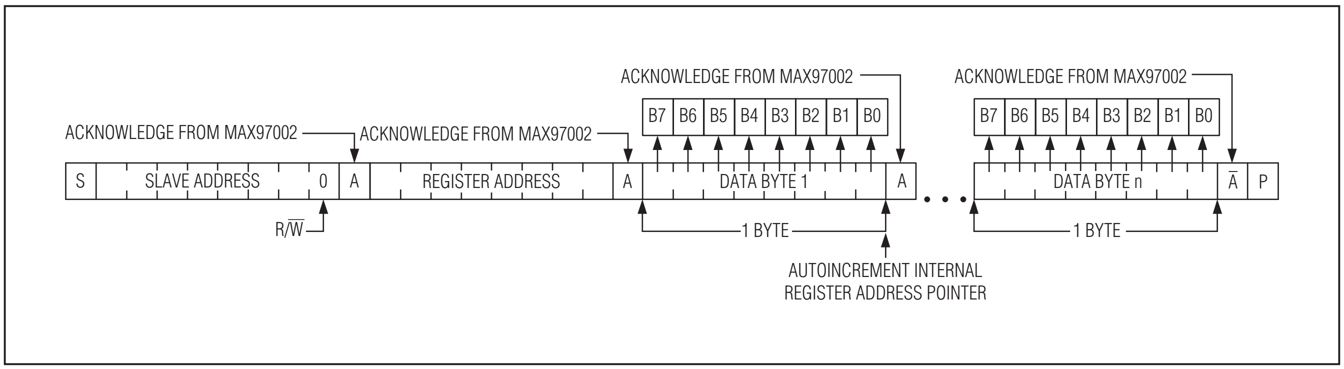


Figure 11. Writing n-Bytes of Data to the MAX97002

Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX97002 acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START (S) command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX97002 is the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP (P) condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX97002's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START (Sr) condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX97002 then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 12 illustrates the frame format for reading one byte from the MAX97002. Figure 13 illustrates the frame format for reading multiple bytes from the MAX97002.

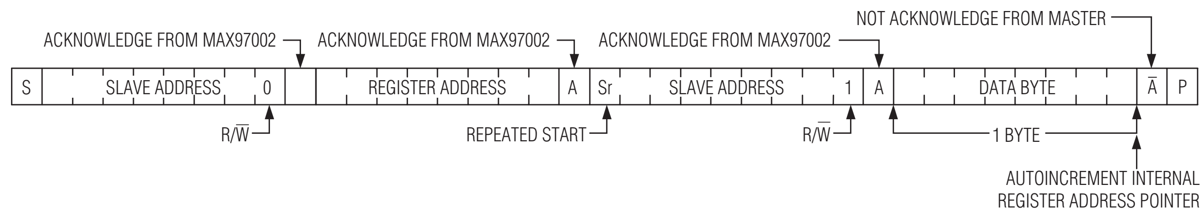


Figure 12. Reading One Byte of Data from the MAX97002

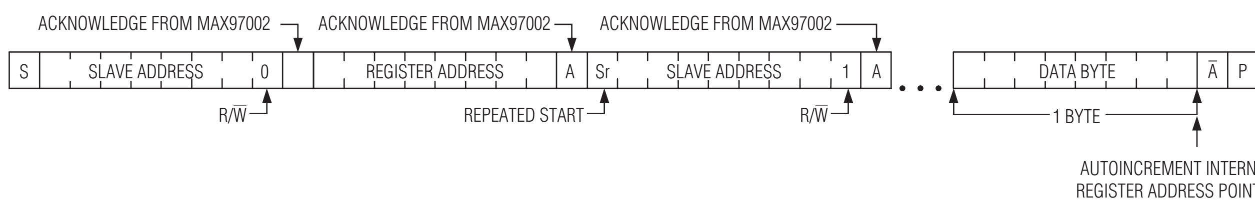


Figure 13. Reading n-Bytes of Data from the MAX97002

Applications Information

Filterless Class D Operation

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filters add cost, increase the solution size of the amplifier, and can decrease efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings (2 x $V_{DD(P-P)}$) and causes large ripple currents. Any parasitic resistance in the filter components results in a loss of power, lowering the efficiency.

The MAX97002 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminating the output filter results in a smaller, less costly, more efficient solution.

Because the frequency of the MAX97002 output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum results, use a speaker with a series inductance > 10µH. Typical 8Ω speakers exhibit series inductances in the 20µH to 100µH range.

RF Susceptibility

GSM radios transmit using time-division multiple access (TDMA) with 217Hz intervals. The result is an RF signal with strong amplitude modulation at 217Hz and its harmonics that are easily demodulated by audio amplifiers. The MAX97002 is designed specifically to reject RF signals; however, PCB layout has a large impact on the susceptibility of the end product.

In RF applications, improvements to both layout and component selection decreases the MAX97002's susceptibility to RF noise and prevent RF signals from being demodulated into audible noise. Trace lengths should be kept below 1/4 of the wavelength of the RF frequency of interest. Minimizing the trace lengths prevents them from functioning as antennas and coupling RF signals into the MAX97002. The wavelength (λ) in meters is given by:

$$\lambda = c/f$$

where c = 3 x 10^8 m/s, and f = the RF frequency of interest.

Route the audio signals on the middle layers of the PCB to allow the ground planes above and below to shield them from RF interference. Ideally, the top and bottom layers of the PCB should primarily be ground planes to create effective shielding.

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

Additional RF immunity can also be obtained from relying on the self-resonant frequency of capacitors as it exhibits the frequency response similar to a notch filter. Depending on the manufacturer, 10pF to 20pF capacitors typically exhibit self resonance at RF frequencies. These capacitors when placed at the input pins can effectively shunt the RF noise at the inputs of the MAX97002. For these capacitors to be effective, they must have a low-impedance, low-inductance path to the ground plane. Do not use microvias to connect to the ground plane as these vias do not conduct well at RF frequencies.

Component Selection

Optional Ferrite Bead Filter

Additional EMI suppression can be achieved using a filter constructed from a ferrite bead and a capacitor to ground (Figure 14). Use a ferrite bead with low DC resistance, high-frequency (> 600MHz) impedance between 100Ω and 600Ω, and rated for at least 1A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Select a capacitor less than 1nF based on EMI performance.

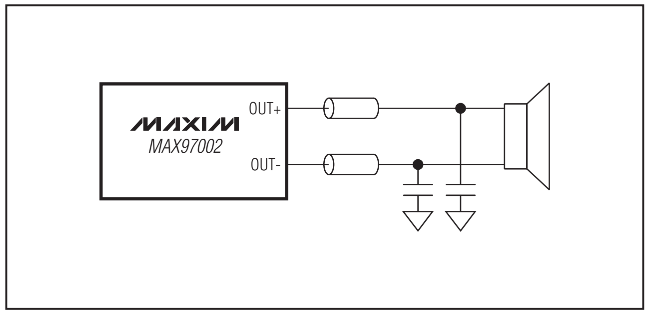


Figure 14. Optional Class D Ferrite Bead Filter

Input Capacitor

An input capacitor, C_{IN}, in conjunction with the input impedance of the MAX97002 line inputs forms a highpass filter that removes the DC bias from an incoming analog signal. The AC-coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. For best audio quality, use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. Most surface-mount ceramic capacitors satisfy the ESR requirement. For best performance over the extended temperature range, select capacitors with an X7R dielectric.

Charge-Pump Flying Capacitor

The value of the flying capacitor (connected between C1N and C1P) affects the output resistance of the charge pump. A value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of the flying capacitor reduces the charge-pump output resistance to an extent. Above 1µF, the on-resistance of the internal switches and the ESR of external charge-pump capacitors dominate.

Charge-Pump Holding Capacitor

The holding capacitor (bypassing HPVDD and HPVSS) value and ESR directly affect the ripple on the supply. Increasing the capacitor's value reduces output ripple. Likewise, decreasing the ESR reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Load Resistance graph in the *Typical Operating Characteristics* for more information

Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. Use a large continuous ground plane on a dedicated layer of the PCB to minimize loop areas. Connect GND directly to the ground plane using the shortest trace length possible. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any digital noise from coupling into the analog audio signals.

Place the capacitor between C1P and C1N as close to the MAX97002 as possible to minimize trace length from C1P to C1N. Inductance and resistance added between C1P and C1N reduce the output power of the headphone amplifier. Bypass HPVDD and HPVSS with capacitors located close to the pins with a short trace length to GND. Close decoupling of HPVDD and HPVSS minimizes supply ripple and maximizes output power from the headphone amplifier.

Bypass PVDD to GND with as little trace length as possible. Connect OUTP and OUTN to the speaker using the shortest and widest traces possible. Reducing trace length minimizes radiated EMI. Route OUTP/OUTN as a differential pair on the PCB to minimize the loop area, thereby reducing the inductance of the circuit. If filter components are used on the speaker outputs, be sure to locate them as close as possible to the MAX97002 to ensure maximum effectiveness. Minimize the trace length from any ground tied passive components to GND to further minimize radiated EMI.

An evaluation kit (EV kit) is available to provide an example layout for the MAX97002. The EV kit allows quick setup of the MAX97002 and includes easy-to-use software, allowing all internal registers to be controlled.

WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and the recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications* on Maxim's website at **www.maxim-ic.com/ucsp**. See Figure 15 for the recommended PCB footprint for the MAX97002.

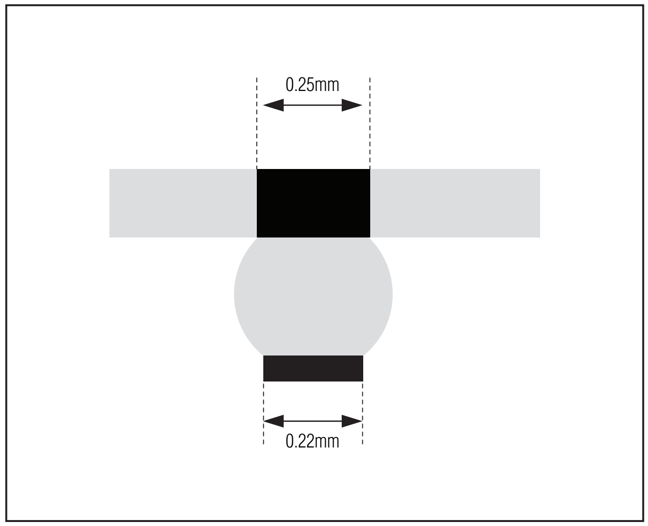


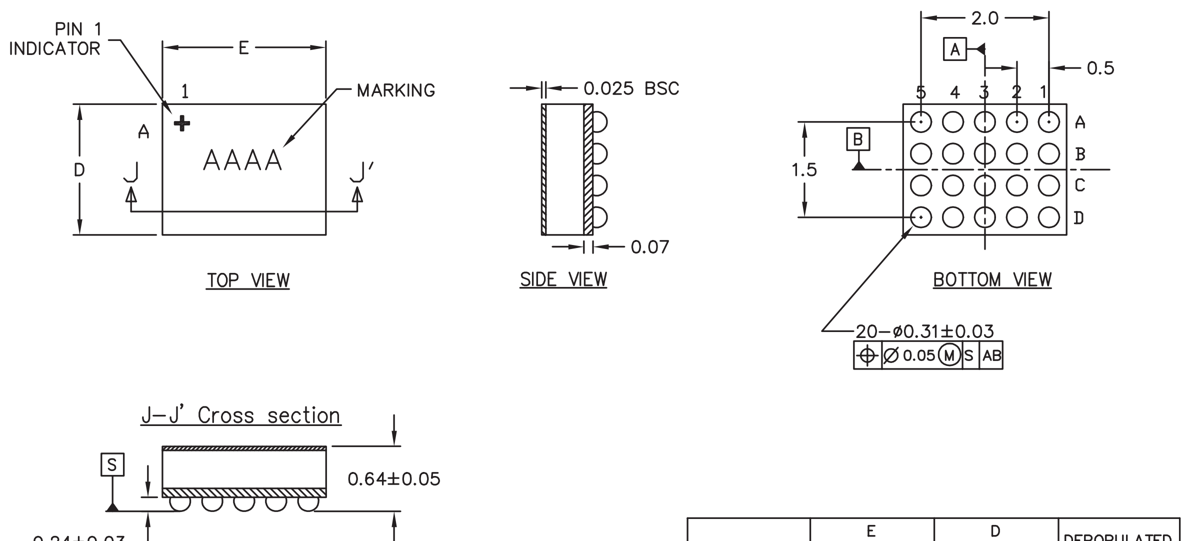
Figure 15. Recommended PCB Footprint

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 WLP	W202A2+2	21-0059	—



PKG. CODE	E MIN	E MAX	D MIN	D MAX	DEPOPULATED BUMPS
W202A2+1	2.47	2.60	1.96	2.09	B3, C3
W202A2+2	2.49	2.62	1.98	2.11	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.

−DRAWING NOT TO SCALE−

TITLE:		
PACKAGE OUTLINE 20L WLP PKG. (5x4) 0.5mm PITCH		
APPROVAL	DOCUMENT CONTROL NO. 21−0059	REV. A 1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/10	Initial release	—
1	7/10	Corrected mixer bit descriptions	25